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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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In re Applicant:	LESTER J. KOZLOWSKI FRANK CHUNG WU-JING HO	Art Unit:	
Filed:	April 24, 2000		
Serial No.:	09/557,454	Examiner:	
For:	JFET/CMOS IMAGER	Docket No.:	98RSS367

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Applicants hereby submit the following references in accordance with 37 C.F.R. §§ 1.56 and 1.97. Copies of the references cited in the attached PTO-1449 are enclosed.

Respectfully submitted,

David R. Clonts, Reg. No. 36,768

Date: 6/15/00

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to the Commissioner for Patents, Washington, D.C. 20231 on June 15, 2000.

David R. Clonts, Reg. No. 36,768

FACSIMILE OF FORM PTO-1449 (REV. 6-89)	U.S. DEPARTMENT OF COMMERCE Patent and Trademark Office	ATTORNEY'S DOCKET NUMBER 98RSS367	SERIAL NUMBER 09/557,454
		APPLICANTS Lester J. Kozlowski et al.	
INFORMATION DISCLOSURE CITATION (Use Several Sheets if Necessary)		FILING DATE April 24, 2000	GROUP ART UNIT

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JUL 26 2000
Group 2700

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	AA	*CMOS: Circuit Design, Layout, and Simulation*; R. Jacob Baker, Harry W. Li and David E. Boyce, 1998, Chpt. 2-4.
	BB	*Integrated Circuit Manufacturability, The Art of Process and Design Integration*, Dhiraj K. Pradhan, 1999, Chpt. 4-5.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the patent owner.